Transient Voltage Suppressors for ESD Protection

General Description

The ESD9B Series is designed to protect voltage sensitive components from ESD. Excellent clamping capability, low leakage, and fast response time provide best in class protection on designs that are exposed to ESD. Because of its small size, it is suited for use in cellular phones, MP3 players, digital cameras and many other portable applications where board space comes at a premium.

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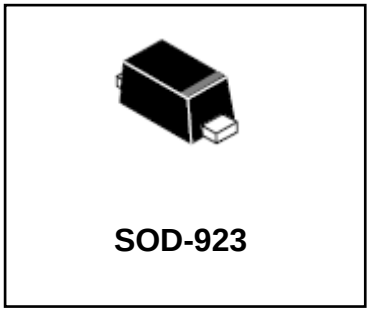

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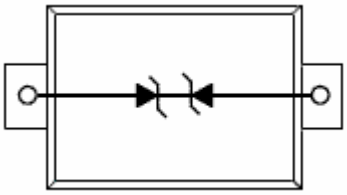

We declare that the material of product compliance with RoHS requirements.

Specification Features

- Low Capacitance 15 pF
- Low Clamping Voltage
- Small Body Outline Dimensions: 0.039″ x 0.024″ (1.0mm x 0.60mm)
- Low Body Height: 0.016″ (0.4 mm)
- Stand−off Voltage: 3.3 V, 5 V
- Low Leakage
- Response Time is < 1 ns
- IEC61000−4−2 Level 4 ESD Protection
- AEC−Q101 Qualified and PPAP Capable
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements
- This is a Pb−Free Device

Mechanical Characteristics

CASE: Void-free, transfer-molded, thermosetting plastic
Epoxy Meets UL 94 V−0
LEAD FINISH: 100% Matte Sn (Tin)
MOUNTING POSITION: Any
QUALIFIED MAX REFLOW TEMPERATURE: 260°C
Device Meets MSL 1 Requirements

Ordering information

Device	Marking	Shipping
LESD9B5.0ST5G	M	8000/Tape&Reel

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IEC 61000−4−2 (ESD) Contact Air		±18 ±18	kV
IEC 61000−4−4 (EFT)		40	A
Total Power Dissipation on FR−5 Board (Note 1) @ T_A = 25°C	P_D	300	mW
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	400	°C/W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Second Duration)	T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. FR−5 = 1.0 x 0.75 x 0.62 in.

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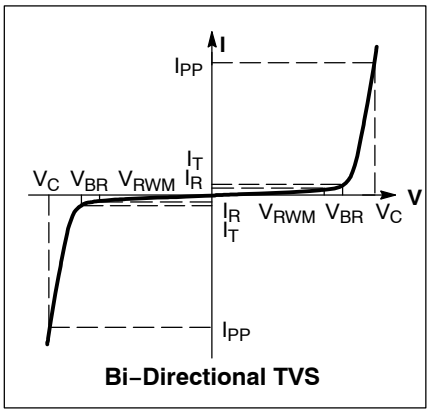
ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
C	Capacitance @ V_R = 0 V and f = 1.0 MHz



Bi−Directional TVS

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Device	Device Marking	V_{RWM} (V)	I_R (μA) @ V_{RWM}	V_{BR} (V) @ I_T (Note 2)		I_T	C (pF)	V_C	V_C (V) @ I_{PP} = 1 A
		Max	Max	Min	Max	mA	Typ	Per IEC61000−4−2 (Note 3)	Max Per 8 x 20 μs (Note 4)
LESD9B5.0ST5G	M	5.0	1.0	5.8	7.8	1.0	15	Figures 1 and 2 See Below	12.5

2. V_{BR} is measured with a pulse test current I_T at an ambient temperature of 25°C.
3. For test procedure see Figures 3 and 4 and Application Note AND8307/D.
4. Surge current waveforms per Figure 5.

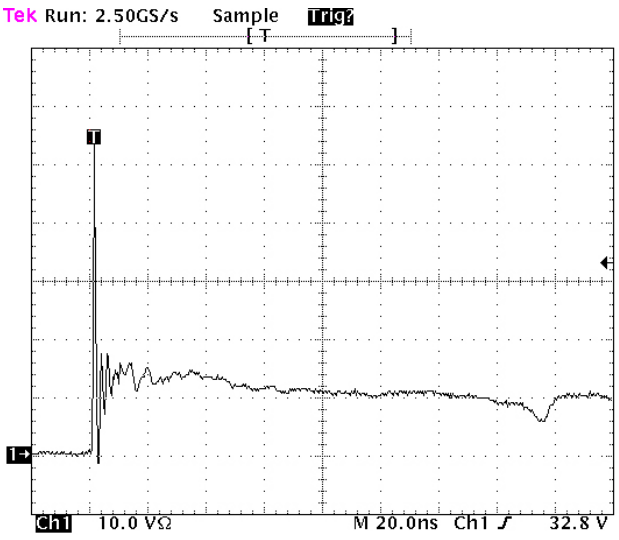


Figure 1. ESD Clamping Voltage Screenshot
Positive 8 kV Contact per IEC61000−4−2

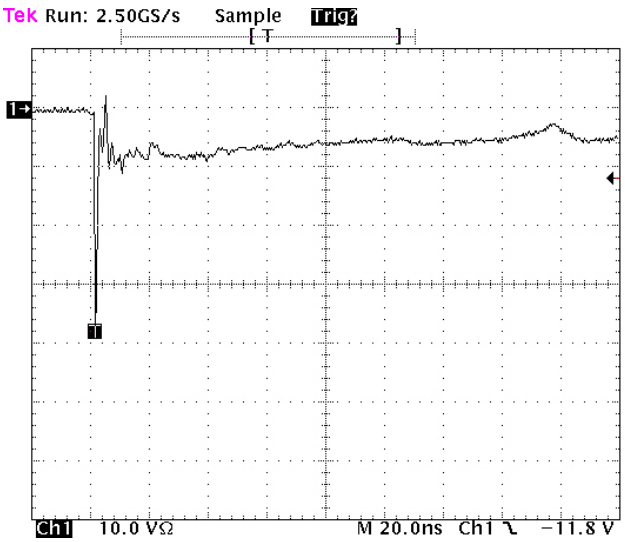


Figure 2. ESD Clamping Voltage Screenshot
Negative 8 kV Contact per IEC61000−4−2

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IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

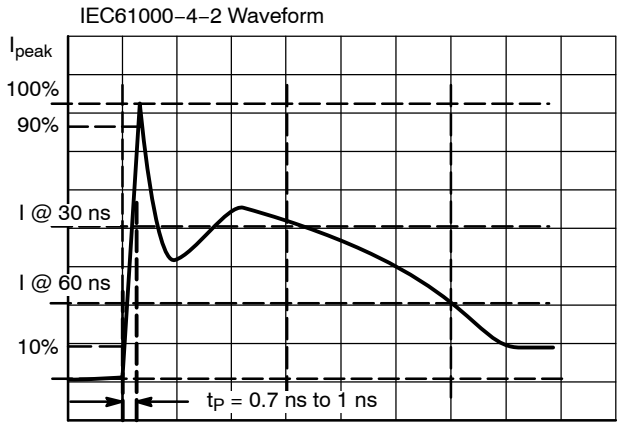

Figure 3. IEC61000−4−2 Spec

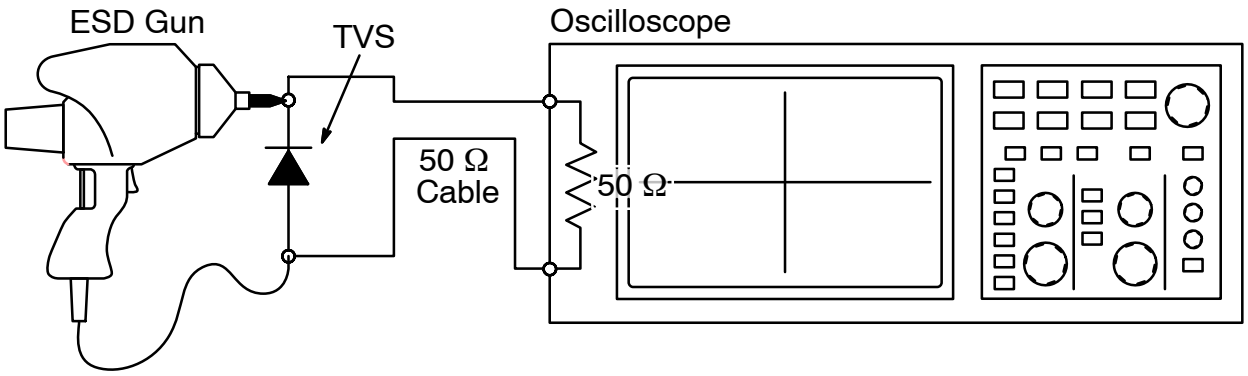

Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

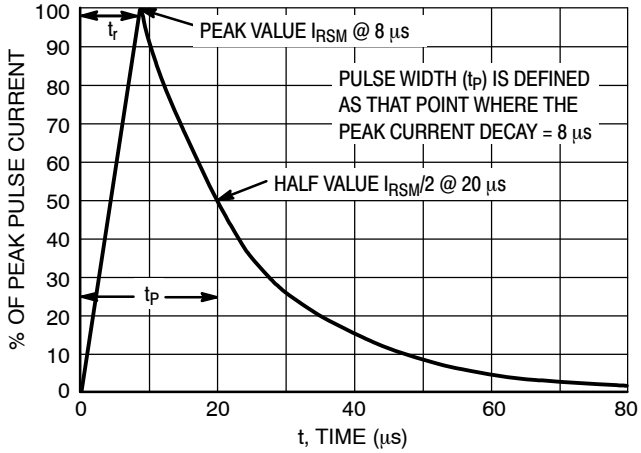

Figure 5. 8 X 20 μs Pulse Waveform

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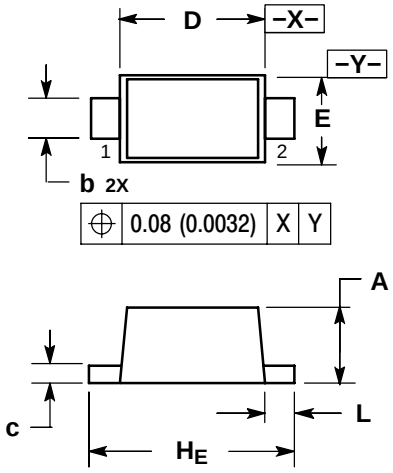

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.34	0.37	0.40	0.013	0.015	0.016
b	0.15	0.20	0.25	0.006	0.008	0.010
c	0.07	0.12	0.17	0.003	0.005	0.007
D	0.75	0.80	0.85	0.030	0.031	0.033
E	0.55	0.60	0.65	0.022	0.024	0.026
H_E	0.95	1.00	1.05	0.037	0.039	0.041
L	0.05	0.10	0.15	0.002	0.004	0.006

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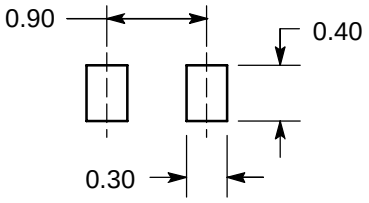

DIMENSIONS: MILLIMETERS